UNIVERSITY OF KWAZULU-NATAL

School of Engineering: Electrical, Electronic & Computer Engineering

MAIN EXAMINATIONS: November 2013

Course and Code: **Electrical Principles 2: ENEL2EB H2**

Duration: THREE hours **Paper 1 of 1** **Total marks: 100**

Examiners:	Mr. H Jay	(Analogue Electronics)
	Mr. E Bhero	(Digital Electronics)
Independent Moderator:	Prof. S H Mneney	

General Instructions:

1. This paper contains two sections, **Analogue Electronics** and **Digital Electronics.**
2. Answer each section in a **separate answer book**. Note the name of the section on the front cover of the answer book.
3. Answer **ALL** questions in both sections.
4. You may use any calculator, provided that no text or formulae are present in memory at the start of the examination.
5. **No notes** of any form are allowed in the examination.
6. Show all working in calculations and derivations.
7. Fully label all diagrams and graphs.

Examination Sub-minimum Requirement:

Students must obtain a sub-minimum of 40% in the Analogue section and 40% in the Digital section of the examination.

ANALOGUE ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question A1 [20 marks]

A1.1.1 Design a single op-amp circuit to produce an output voltage $V_o = -(10 \cdot V_1 + 15 \cdot V_2 + 27 \cdot V_3)$ from three input signals V_1, V_2 & V_3. Assume the op-amp is ideal, calculate the resistances required if the minimum resistance to be used is 10 kΩ, and draw the circuit diagram. [3]

A1.1.2 This circuit is then constructed using an op-amp with the following specifications:

input bias current = 500 nA (max.); input offset current = 200 nA (max.);
input offset voltage = ±6 mV (max.); unity-gain frequency = 2 MHz;
slew-rate = 0,5 V/μs

Determine the maximum dc output voltage expected from this circuit if the inputs are grounded. [2]

A1.2 The audio amplifier circuit in Figure A1 uses the same op-amp as in Question A1.1.2 above.

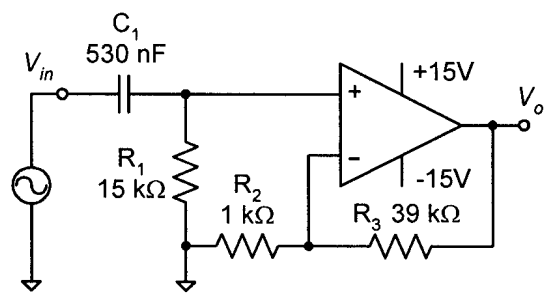

Figure A1

A1.2.1 Determine the voltage gain $A_V = V_o / V_{in}$ (in dB) at "mid-band" frequencies where the capacitor reactance is negligible. Determine the relevant corner frequencies for this amplifier and hence determine the transfer function $TF = V_o / V_{in}$ as a function of frequency and thus sketch the Bode magnitude form of frequency response showing relevant numerical details. [6]

A1.2.2 Briefly explain what is meant by the term *Full Power Bandwidth* (FPBW) of an op-amp, and calculate the FPBW for this op-amp operating in this circuit. [2]

A1.2.3 While testing this amplifier, a student applies a sinusoidal input voltage V_{in} of 150 mVrms at a frequency of 12 kHz and monitors the input and output signals with an oscilloscope. Briefly explain (with relevant calculations and sketches) what output waveform would be observed. [3]

A1.3 In order to increase road safety by reducing the overloading of trucks, a municipality installs a vehicle weighbridge on the main roadway. An Instrumentation Amplifier (IA) is used to amplify the load signal from the straingauge load sensor. At maximum load, the sensor produces a full-scale signal of 20 mV which is input to the IA to produce a corresponding output of 10 V full-scale.

The system specification requires that a common mode noise voltage of up to 5 V be tolerated at the input to the IA and that the error so introduced is to be less than 0,05% of full-scale output. An IA with a CMRR specification of 120 dB is available. Define the term represented by CMRR and determine if this IA will be adequate to meet the system specification. [4]

Question A2 [12 marks]

A2. A student is loaned a regulated dc power supply and decides to attempt to build a similar unit. She notes that the circuit comprises a step-down transformer, silicon bridge rectifier, filter capacitor C, and a shunt regulator using series resistor R_S and a Zener diode.
No component values are visible, and the student only has a digital multimeter available. With the transformer primary winding connected to the 230 Vrms 50 Hz ac mains supply the secondary voltage reads 10,2 Vrms. Assume the bridge rectifier diodes each have a forward voltage V_D of 0,7 V when conducting. With no external load connected to this power supply, the capacitor voltage reads 12 Vdc and the output voltage reads 6 Vdc. With this power supply disconnected from the mains, series resistor R_S measures 100 Ω.

A2.1 Draw the circuit diagram of this supply labelling relevant voltages and currents. Determine the capacitance value, the power dissipated in R_S and the Zener diode voltage and power rating required assuming the Zener diode average current should be limited by R_S to 80% of the maximum rated value. [6]

A2.2 Determine the diode conduction angle in degrees, the peak diode currents and the PIV rating required for the bridge rectifier diodes. Hence simply sketch the capacitor voltage and diode current waveforms expected showing relevant numerical values. [5]

A2.3 From the data sheet for a suitable Zener diode, the student finds that the dynamic Zener resistance r_Z is typically 5 Ω. Determine the expected ripple voltage at the output of the supply with no load. [1]

Question A3 [18 marks]

A3. A 2-stage BJT amplifier circuit is shown in Figure A2 below.

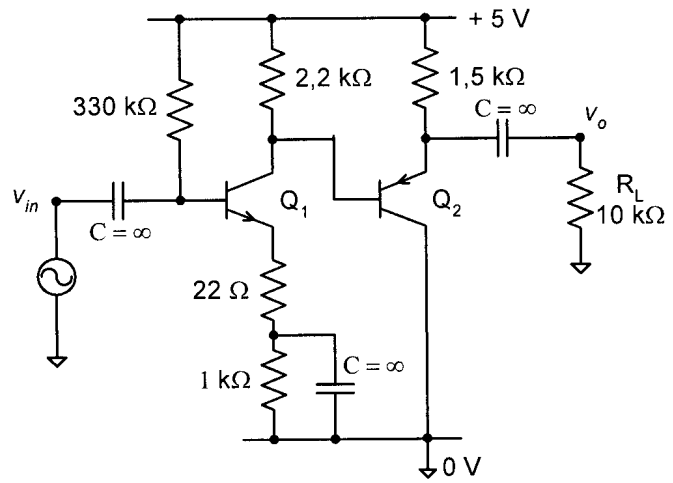

Figure A2

A3.1 Assuming V_{BE} = 0,7 V and β = 100 for the BJTs, determine the dc collector current I_{C1} of Q_1 and assuming $I_{B2} << I_{C1}$, determine the emitter current I_{E2} of Q_2. Determine V_{CE1} and V_{CE2} and hence determine if the BJTs are in active mode. [5]

A3.2 Identify the transistor configuration for each BJT and draw a small-signal equivalent circuit for this amplifier using appropriate BJT models assuming V_T = 25 mV and $V_A = \infty$. Determine the voltage gain $A_v \equiv v_o / v_{in}$ (in dB) assuming the capacitor reactances are negligible at signal frequencies. [8]

A3.3 Identify the transistor amplifier configuration in the circuit in Figure A3. Hence design the dc bias circuit to operate the BJT at $I_C \approx 2$ mA assuming $\beta = 250$, $V_{BE} = 0{,}7$ V in active mode, and $V_A = \infty$. Show all design calculations and select nearest E12 standard resistor values (see below). [5]

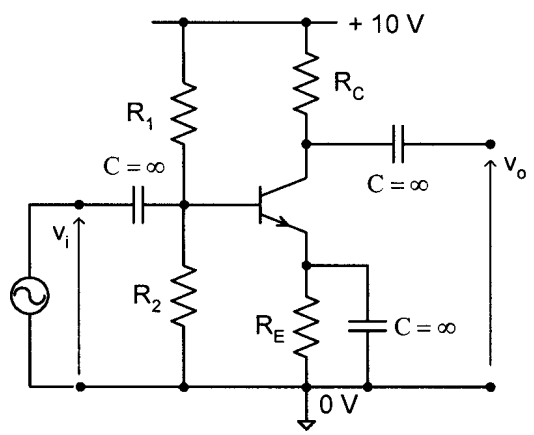

Figure A3

E12 series:	10	12	15	18	22	27	33	39	47	56	68	82

End of Analogue Electronics

DIGITAL ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question D1 [25 marks]

D1.1 *Parity-bits* are normally used as error-detection codes. A *three-bit word* communication system requires an *even-bit parity generator*.

D1.1.1 Write down the truth table for the *even-bit parity generator.*
D1.1.2 Hence, draw implementation logic for this *even-bit parity generator.*

[2+4]

D1.2 Using Karnaugh map procedure, show that:

a) $F = \bar{W}X + W\bar{X}\,\bar{Y} + WX\bar{Y}Z + \bar{X}YZ + \bar{Y}\bar{Z} + \bar{W}\bar{X}\,\bar{Y}Z = \bar{Y} + \bar{W}X + \bar{X}Z$
b) Hence, implement, $F = \bar{Y} + \bar{W}X + \bar{X}Z$, using NAND gates **only**.

[5+4]

D1.3 Figure D1 shows the complementary metal-oxide semiconductor (CMOS) transistor implementation of a particular logic function.

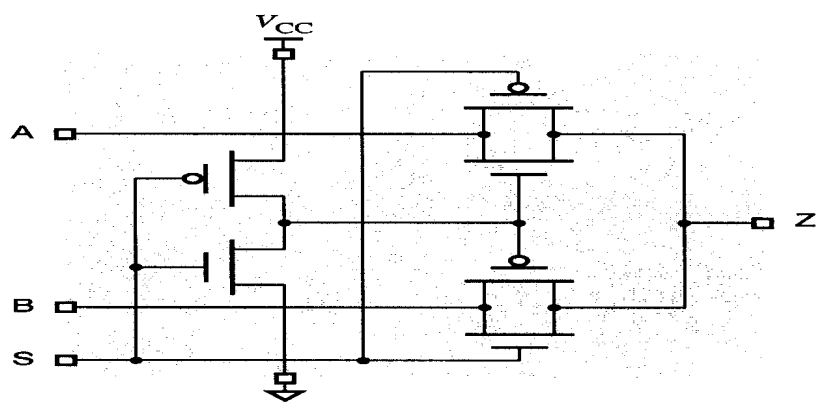

Figure D1

D1.3.1 Given that *A*, *B* and *S* are inputs and *Z* is the output, write down the circuit truth table. [4]

D1.3.2 Based on the truth table, derive a simplified logic expression for *Z*. [2]

D1.3.3 Determine the output bit-stream if the input bit-streams *A=1011*, *B=1101* and *S=1100* are applied to the circuit. [1]

D1.4 A 4-bit binary weighted resistor DAC has R=1.4KΩ with a reference voltage of 9V. Given that the load resistance = 330Ω, what is the output voltage if the binary input is 1010?

[3]

Question D2: [25 marks]

D2.1 Implement the following Boolean function with a Multiplexer:

$$F(A,B,C,D) = \prod(4,5,6,7,11,12,13,14,15)$$

[5]

D2.2 Draw a logic circuit diagram for a T flip-flop and write down its truth table.

[4]

D2.3 Using MSI chips and any logic gates of your choice, design a counter which counts up and down continuously from 0 to 99 then down to 0. The count must be displayed on **two** 7-segment LED displays. In your answer, you should:

i. State any assumptions made in your design.
ii. Give a complete block diagram of the system.
iii. Give brief explanation on how the system works.

[8]

D2.4 Design a 4-bit shift register, which can load or output a 4-bit word in serial or parallel format. Given a 4-bit word, 1101, answer the following questions:

i. If the word, 1101, is to be loaded serially, draw the timing diagram **and** state the sequence of steps *(control signals)* required to complete this loading process.
ii. If the word, 1101, is to be loaded in parallel, state the sequence of steps *(control signals)* required to complete this loading process.

[4+3+1]

End of Digital Electronics