UNIVERSITY OF KWAZULU-NATAL
School of Engineering

MAIN EXAMINATIONS: 2013

Subject, Course and Code: **Electronic Engineering: ENEL2ECH2**

Duration: TWO hours **Paper 1 of 1** **Maximum marks: 60**

Examiners: Mr. R Sewsunker (Internal)
Prof. T J O Afullo (Independent Moderator)

Instructions:

1. **Answer BOTH questions in Section A and ANY ONE question in Section B.**
2. Show adequate work in your solutions.
3. **No notes** of any form are allowed in the examination.
4. Programmable calculators may be used, provided **text and formulae are removed from memory prior to the start of the examination.**
5. Label all sketches and plots.

SECTION A: Answer BOTH questions in this Section.

Question A1: [20 marks]

(a) The circuit shown in Figure 1 uses real diodes each of which has a forward voltage drop of 0.8 Volts.

(i) Show with justification the assumption that both diodes are ON is incorrect. [3]

(ii) Determine the correct states of the diodes supporting your answers with justification. [2]

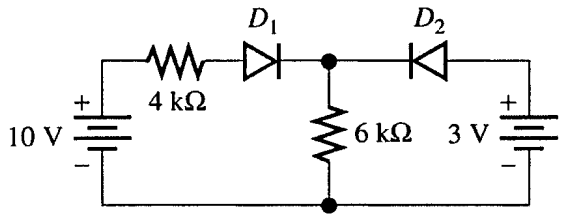


Figure 1

(b) The circuit in Figure 2 is based on a real operational amplifier which has a maximum input offset voltage of 10 mV. Given that $\frac{R_2}{R_1} = 10$, determine the maximum output error voltage. [3]

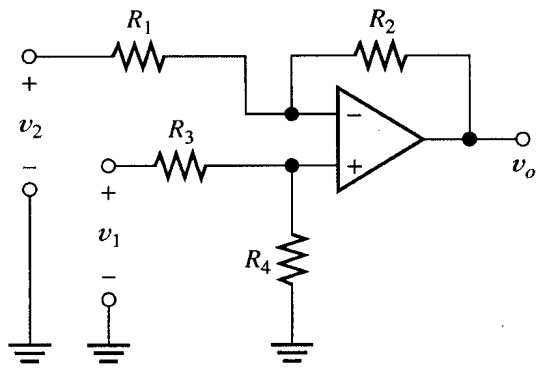


Figure 2

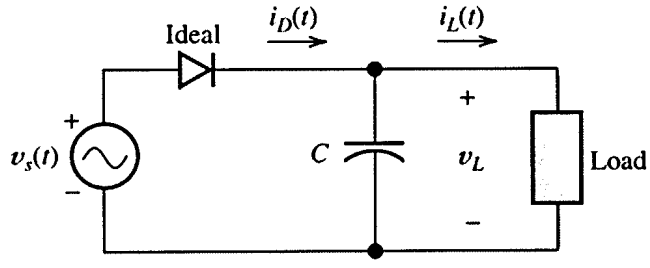
(c) The following logic problem is posed. A hydroponic tomato bed is monitored by three sensors as follows: level of nutrition, *N* = logic 1 provided the nutrition level is sufficient; water level, *W* = logic 1 provided the water level is sufficient and temperature alert, *T* = logic 0 if the bed temperature is within limits.

(i) Draw the truth table and write down the simplified logic expression for the logic function of an alarm signal, $A = f(N,W,T)$ which sounds a buzzer if either both the water and nutrition levels are low or the temperature is out of limits. [2]

(ii) Draw the logic circuit diagram that implements $A = f(N,W,T)$ [1]

(iii) Draw an alternate logic circuit diagram for $A = f(N,W,T)$ using only NAND gates. [2]

(d) Consider the half-wave rectifier based power supply circuit shown in Figure 3, designed to have a peak-to-peak ripple voltage of 2 V.
In the circuit $v_S(t) = 20\sin(200\pi t) volts, R_{Load} = 190\Omega.$



$$C = \frac{I_L T}{V_{r(peak-to-peak)}}$$

Figure 3

(i) Sketch the voltage waveform across the load resistor for one cycle of the input signal, showing the peak value. [2]
(ii) Calculate the average value of the voltage across the load. [1]
(iii) Given the expression for *C* as shown above, compute the capacitance value needed. [2]
(iv) How would the peak-to-peak ripple voltage change if the half-wave rectifier diode in the circuit is replaced by full-wave diode-bridge based rectifier, also made up of ideal diodes? What would happen to the average value of the load current? [2]

Question A2: [20 marks]

(a) A simple BJT amplifier is shown in Figure 4. The BJT has $\beta = 100$ and $V_{BE} = 0.7V$.

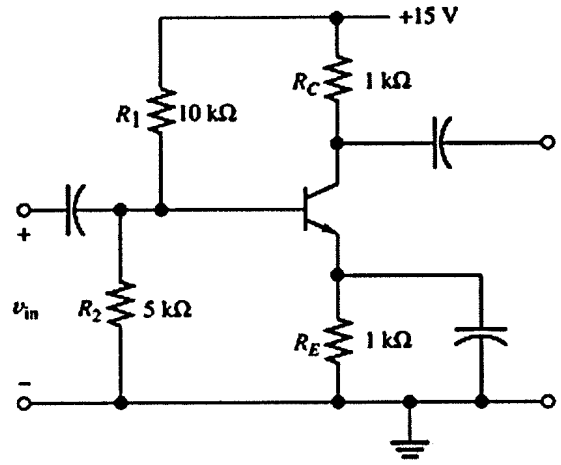
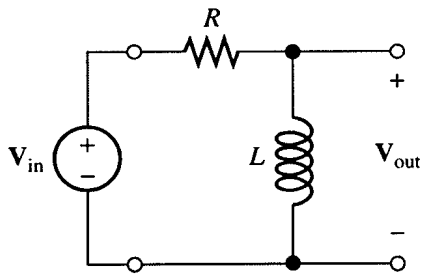


Figure 4

(i) Analyse the dc bias circuit to determine I_C and V_{CE}. [6]
(ii) Confirm the BJT is in the correct region for amplifier operation. [1]

(b) Figure 5 shows the circuit of a filter with $L = 10\mu H$, $R = (20\pi)\Omega$.



[Impedance, $Z_L = j\omega L$]

Figure 5

(i) Find the circuit transfer function, *H(f)*. [2]

(ii) Draw the asymptotic Bode magnitude and phase plots for the circuit. [6]

(c) Figure 6 shows a 4-bit digital-to-analog converter (DAC) based on an operational amplifier. In the circuit if the input bit is 1, the corresponding switch is up; if the bit is 0 the switch is down. Let the binary input be represented by $b_3b_2b_1b_0$, where b_3 controls S_3, b_2 controls S_2, etc.

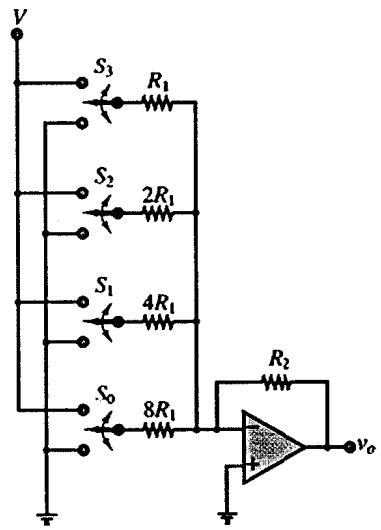


Figure 6

(i) Using values of 100 kΩ for R_1, 50 kΩ for R_2, and 1 volt for V, solve for the analog output for input $b_3b_2b_1b_0 = 0110$. Assume all components of the circuit, the voltage source V and the ground connection are ideal. [3]

(ii) The above circuit produces an analog output with ±2 % full-scale error. Comment on the match of resolution and accuracy for this DAC. Support your answer with reason. [2]

SECTION B: Answer ANY ONE question in this Section.

Question B1: [20 marks]

(a) Figure 7 shows a circuit based on an ideal operational amplifier and a signal used as input to the circuit.

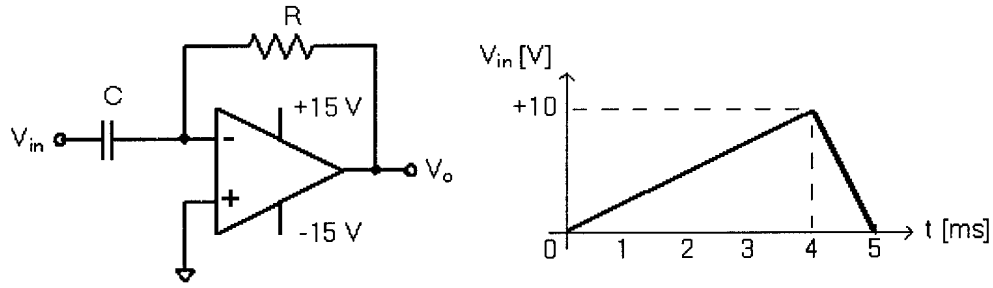


Figure 7

(i) Identify the circuit and from first principles solve for the output voltage in terms of the input voltage. [3]

(ii) Given $R = 5k\Omega, C = 200nF$ draw the output voltage waveform for the same period of time as the input signal showing necessary calculations. [4]

(b) Figure 8 shows the complementary metal-oxide semiconductor (CMOS) transistor implementation of a particular logic function.

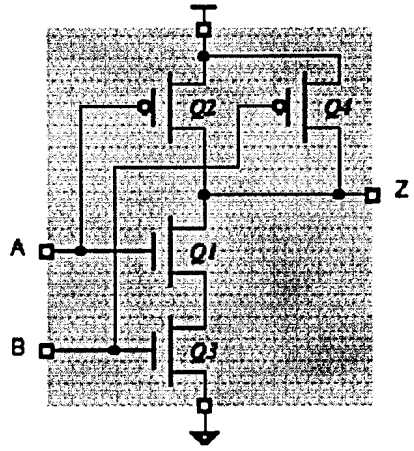


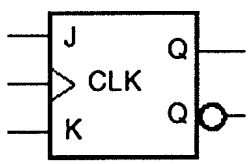
Figure 8

(i) Given that A and B are inputs and Z is the output, draw the equivalent circuit for each input combination based on the switch-model and show the output logic level in each case. [4]

(ii) State what logic function this circuit performs. [1]

(iii) Determine the output bit-stream if the input bit-streams *A=1001* and *B=1101* are applied to the circuit. [1]

(c) Figure 9 shows the circuit symbol of a J-K flip-flop with its function table alongside.



J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

Figure 9

(i) Show how you would connect up a few J-K flip-flops to make a 3-bit binary counter. You may use any additional combinational logic gate needed. Assume a suitable CLOCK waveform is available. [4]

(ii) Show the count operation of your sequential logic circuit in part (i) by drawing the output waveforms. [3]

Question B2: [20 marks]

(a) The circuit shown in Figure 10 is based on ideal operational amplifiers.

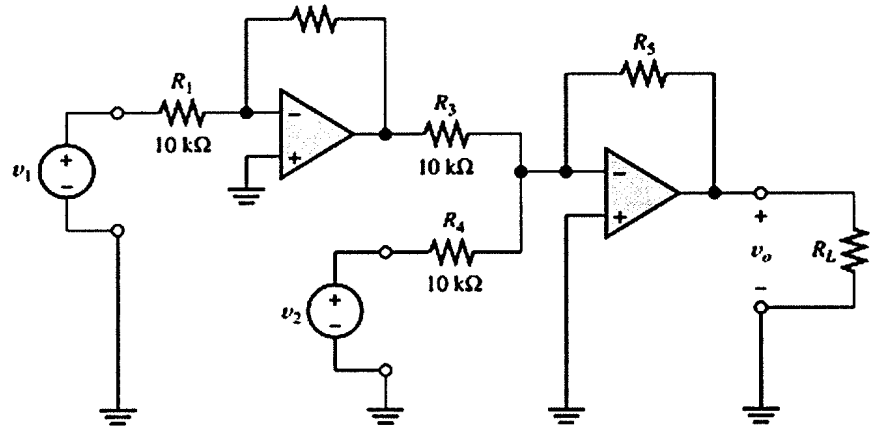


Figure 10

(i) Design the required resistor values so voltage source v_1 sees a voltage gain of +210 and voltage source v_2 sees a voltage gain of -150. [3]

(ii) Assuming 1 % tolerance resistors are available to build the circuit, compute the voltage gain tolerance for each input. [2]

(b) Simplify the following logic expression using basic rules of Boolean algebra. [3]

$$Y = f(A,B) = (A+B)\cdot(\overline{A}+A\cdot B)$$

(c) Figure 11 below shows the circuit of a filter.

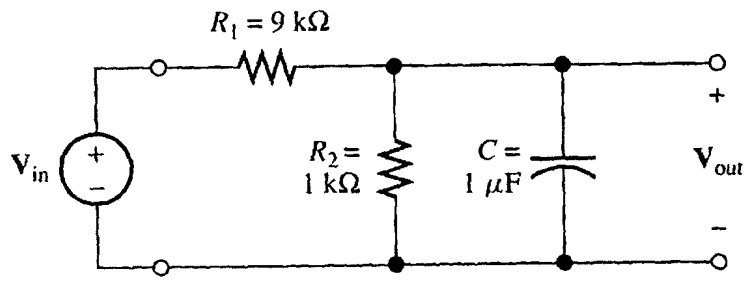


Figure 11

(i) Apply *Thévenins* theorem to draw an equivalent circuit which has a single resistive component. [3]
(ii) Find the circuit transfer function, *H(f)*. [3]
(iii) Draw the asymptotic Bode magnitude and phase plots for the circuit. [6]

END OF EXAM