The Discipline of Electrical, Electronic & Computer Engineering

Main Examination: 3rd October 2013

Embedded Systems (ENEL4ESH2)

Duration: 2 hours **Total Marks 60**

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General Instructions:

1. Answer **all** questions in both Section **A** and Section **B**.
2. You can use a scientific calculator, but clear all program memory.
3. Try to keep your sketches as clear and as readable as possible.

SECTION A

Answer ALL questions in this section in a separate booklet.

Question A1: [15]

NASA space agency wants to develop a space-mission robot called "Ultra-Curiosity (UC)". A hierarchical embedded computer system comprising of one master controller, which is connected to at least four independent slave units will control the UC. Each slave unit is connected to at least four sensors, which sense various environmental parameters such temperature, pressure and so forth. In order to improve the reliability of data sent back to earth, the system implements a voting system that works in the following way; when the master controller broadcasts the parameter to be measured each slave unit will send its own measured value. The value sent by the majority slave units is the one sent back to earth.
Assuming you are the project leader for the UC mission, prepare a design brief to be presented to the technical staff. In your design brief include the following:

a) Labelled block diagram of the system.
b) The type of network connection(s) you are going to use in the UC robot and why you chose that network?
c) The type of Processor(s) you are going to use for your master controller and the slave units and reasons for selecting the chosen processor(s).
d) Write a pseudo code for the possible program running in the master controller.
e) The process design model you are going to use in developing the system and the reasons for choosing that process design model.
f) State any possible design improvements and/or constraints.

[3+2+3+3+2+2]

QuestionA2: [15]

a) Two nodes on an automotive CAN bus are both ready to transmit data but the bus is busy with a message from the headlight switch (HLS) node. The two nodes are the Brake light switch (BLS) and the left indicator switch (LIS) wishing to send messages with IDs 0x023 and 0x07B respectively. Sketch the bus signals from the last bit of the HLS message until only one node is sending. Briefly explain your reasoning in coming up with the sketch. [5]

b) A processor system is in use that comprises 4 different parts. These parts are used 50%, 25%, 10% and 15% of the time respectively. A new system is designed that manages to speed up the sections by 10%, 30%, 5% and 25% respectively. Calculate what the overall system speed-up would be. [5]

c) A single purpose dedicated processor is required that will produce a selected output as per the code loop in Figure A1 below. (*go_i* is a binary input of temperature, the values are presented on the inputs *x_i* and *y_i*. The output is produced on output *d_o*).

```
int x, y, r;
while (1)
{
        while (!go_i);
        x = x_i;
        y = y_i;
        r = (x+y)/2;
        if (r >22) r = 0;
        if (13<= r <=22) r = 7;
        else r = 15;
        d_o = r;
}
```

Figure A1

From Figure A1 above, sketch the logic FSMD diagram for a single purpose processor. [5]

SECTION B

Answer ALL questions in this section in a separate booklet.

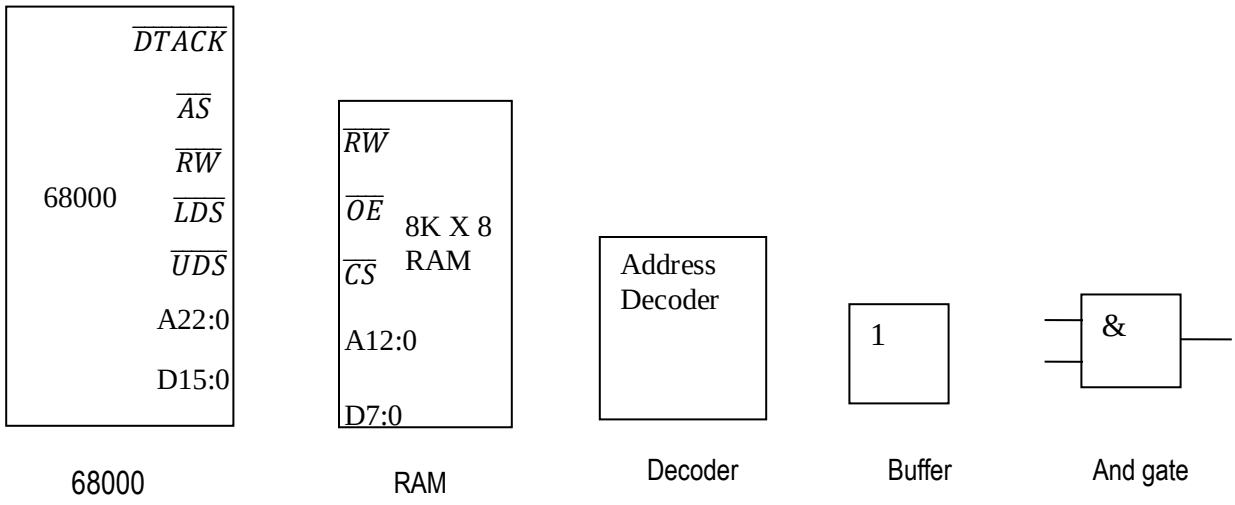
Question B1: Cache memory design and performance [10]

a) Consider a 32 word memory and an 8 word direct mapped cache with a block size of one word. Assume 32-bit words. Determine the size of the tag, index and offset fields for the byte-addressable memory. Determine where memory address 20 maps (i.e. line index). List all memory addresses which map to the same cache block. [10]

Question B2: Memory interfacing [10]

a) You are equipped with the following; a 68000 microprocessor, two 8K X 8 RAM chips, one for holding the upper byte and the second for the lower byte data, an address decoder, a gate and a buffer as shown in Figure B1 below. Draw a full connection diagram for a 68000 microprocessor and the 8K X 8 RAM chips interface. Indicate the sizes of the buses used. You are allowed to use any combination of gates and buffers. [6]

$\overline{\text{UDS}}$	$\overline{\text{LDS}}$	OPERATION	D15:8	D7:0
LOW	LOW	Write word	Upper byte data	Low byte data
LOW	HIGH	Write upper byte	Upper byte data	invalid
HIGH	LOW	Write lower byte	invalid	Low byte data
HIGH	HIGH	No operation	No valid data	No valid data



DTACK → indicates the completion of the data transfer.
AS →Indicated valid address on the bus.

Figure B1. Memory Interfacing

b) Design a basic gate-based address decoder for the interface circuit designed in question B2 a) above that starts from address zero. [4]

Question B3: Peripherals [10]

a) You are required to design a room control system that does the following; starts the fan when the temperature is above a certain threshold and stops it when the temperature is below the threshold, lights a bulb connected to the mains, when there is darkness and vice versa.
   i) Draw the block diagram of the system. [4]
   ii) Determine with reasons the transducers you will use at the input and output. [3]
   iii) Briefly sketch how you will interface to the central controller. [3]

End of Examination Questions