University of KwaZulu Natal

The Discipline of Electrical, Electronic & Computer Engineering

Main Examination: May 2014

Computer Architecture and Organization (ENEL4CO)

Duration: 2 hours **Total Marks: 70**

Examiners: **Internal** Mr. E. Bhero
External Mr. D Bhatt

General Instructions:

1. Answer **all** questions.
2. Scientific calculators may be used with all program memory cleared.
3. Try to keep your sketches as clear and as readable as is possible.

Question 1 (22 Marks)

a) Contemporary processors use various techniques in order to optimize CPU utilization. Describe and explain how the following techniques work:
   1) Branch prediction;
   2) Data flow analysis and;
   3) Speculative execution.

[6]

b) Give a brief comparative account of RISC and CISC computers.

[4]

c) Operand Addressing is one of the important factors in defining instruction set architecture for a computer. Write assembly program to illustrate the impact that the number of operands that can be addressed explicitly has on the program length and execution time. In answering this question, use the arithmetic statement, X = (A+B)(C+D) and separate programs for:
   i. three-address instructions,
   ii. two-address instructions,
   iii. one-address instructions and
   iv. Zero-address instructions.

[12]

Question 2 (28 Marks)

As a design engineer of a new type of a computer system, you want to use a number of 12-bit multiplier integrated chips to build a Floating Point multiplication unit that multiplies two 48-bit floating-point numbers. The inputs to the unit and the output from the unit use floating-point format that gives 12 bits for the exponent and 36 bits for the mantissa. You can use any number of suitable adders in your design. To accomplish this design:

a) Write down the expression that you are going to use to relate the 48-bit floating-point numbers multiplication with the 12-bit words multiplication.

[6]

b) Draw a block diagram of a floating point multiplication unit (without pipelining).

[8]

c) Insert registers at appropriate locations in the block diagram and draw the final pipelined floating point multiplier unit.

[6]

d) If the 12-bit words multiplier needs 75 nanoseconds, the exponent adjustment circuit needs 18 nanoseconds, the addition of the partial products needs 73 nanoseconds, and the propagation and setup time of a register is 14 nanosecond, calculate:

i. The multiplication time without pipelining.
ii. The multiplication time with pipelining.
iii. The speed up ratio.
iv. The data rates of the non-pipelined and the pipelined system.

[8]

Question 3 (20 marks)

a) Using radix 2, multiply the following numbers using Booth's algorithm:

A = -23 and B = -29

[6]

b) Write down the recurrence equation for high-radix multiplication; hence:

Using radix 4, illustrate the multiplication of the numbers, 126 and 237. State the advantages and disadvantages higher radix multipliers.

[6]

c) An IEEE standard for 32-bit floating point numbers has the format:

$$N = -1^{S} \times 1.F \times 2^{E-127}$$

Where S is the sign bit, F is the fractional mantissa, and E is the biased exponent.
By first converting to IEEE format, perform the subtraction 133.5 – 110.25 and express the answer in a packed form.

[8]