UNIVERSITY OF KWAZULU-NATAL

School of Engineering: Electrical, Electronic & Computer Engineering

MAIN EXAMINATIONS: November 2015

Course and Code: **Electrical Principles 2: ENEL2EB H2**

Duration: THREE hours **Paper 1 of 1** **Total marks: 100**

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Independent Moderator:	Prof. T. J. O. Afullo	

General Instructions:

1. This paper contains two sections, **Analogue Electronics** and **Digital Electronics.**
2. Answer each section in a **separate answer book**. Note the name of the section on the front cover of the answer book.
3. Answer **ALL** questions in both sections.
4. You may use any calculator, provided that no text or formulae are present in memory at the start of the examination.
5. **No notes** of any form are allowed in the examination.
6. Show all working in calculations and derivations.
7. Fully label all diagrams and graphs.

Examination Sub-minimum Requirement:

Students must obtain a sub-minimum of 40% in the Analogue section and 40% in the Digital section of the examination.

ANALOGUE ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question A1 [10 marks]

A1.1 What is the highest frequency of a triangle wave of *20 V* peak-to-peak amplitude that can be reproduced by an op amp whose slew rate is *10 V/μs*? For a sine wave of the same frequency what is the maximum amplitude of output signal that remain undistorted? [2+2]

A1.2 Assuming the diodes to be ideal, find the values of I and V in the Fig. A1.2. [2+1]

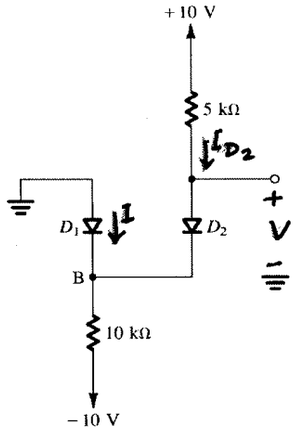

Figure A1.2

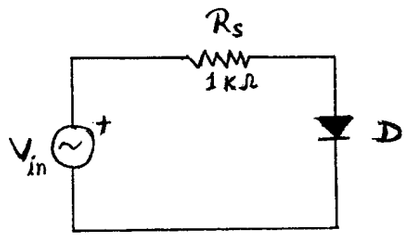

Figure A1.3

A1.3 The source voltage is $v_{in} = 6 + sin(\omega t)$ Volts in the circuit of Fig. A1.3. It is a silicon diode so the barrier potential voltage is still *0.7 V* and assume $\eta=1$. Find the dynamic resistance and Voltage drop through diode. [1+2]

Question A2 [20 marks]

A2.1 The first stage of a two-stage amplifier may be modelled by a voltage amplifier with input resistance $R_{i1} = 12\ k\Omega$, open-circuit voltage gain $A_{Vo} = 50\ V/V$, output resistance $R_{o1} = 2\ k\Omega$ and the second stage may be modelled by a current amplifier with input resistance $R_{i2} = 8\ k\Omega$, short-circuit current gain $A_{Is} = 20\ A/A$, output resistance $R_{o2} = 15\ k\Omega$.

Draw a labelled circuit diagram of this two-stage amplifier and hence determine a single transconductance amplifier model for it. [2+2]

The amplifier is now fed from a voltage source V_s with source resistance $R_s = 3\ k\Omega$ and the output is connected to a load resistance $R_L = 3\ k\Omega$. Draw a labelled circuit diagram of this transconductance amplifier and hence determine the overall voltage gain $A_{Vs} \equiv V_o / V_s$ where V_o is the output voltage. [1+3]

A2.2 Assuming the op-amp to ideal, derive an expression for the closed-loop gain v_o/v_i of the circuit shown in Fig. A2.2. Use this circuit to design (means to find the approx. value of R_1, R_2, R_3, and R_4) an inverting amplifier with a gain of *100* and an input resistance of *1 MΩ*. Assume that for the practical reason it is required not to use resistors greater than *1 MΩ*.[6+2]

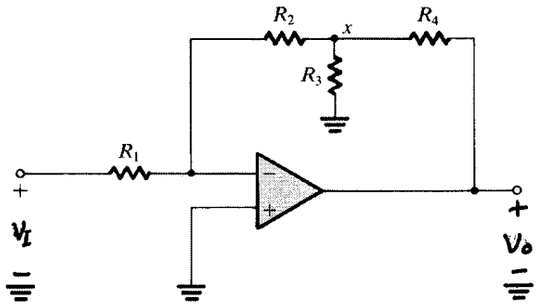

Figure A2.2

A2.3 An op-amp based inverting integrator is measured at *1 kHz* to have a voltage gain of *(-100 V/V)*. At what frequency is its gain reduced to *(-1 V/V)* ? [2]
What is the integrator time constant? [2]

Question A3 [20 marks]

A3.1 A Common-Emitter amplifier utilizes a BJT with $\beta = 100$ and $V_A = 100\ V$, is biased at $I_C = 1\ mA$ and has a collector resistance $R_C = 5\ k\Omega$. Find the R_{in}, R_o, and A_{vo}. [1+1+2]

If the amplifier is fed with a signal source having a resistance of *5 kΩ* and a load resistance $R_L = 5\ k\Omega$ is connected to the output terminal, find the resulting A_v and G_v. [3+3]

A3.2 A 2-stage BJT amplifier circuit is shown in Fig A3.2 below.

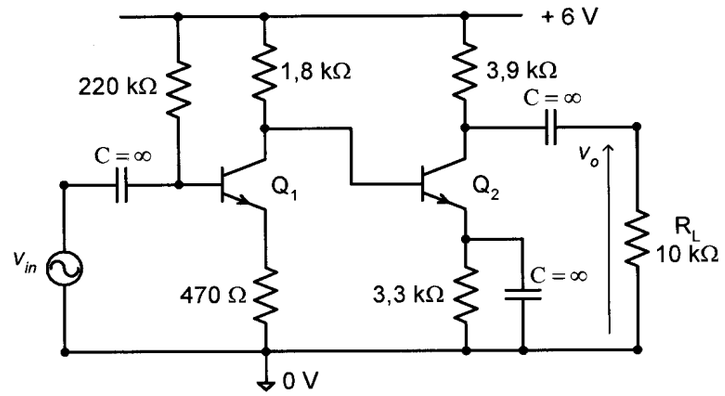

Figure A3.2

A3.2.1 Assuming $V_{BE} = 0.7\ V$ and $\beta = 100$ for the BJTs, determine the dc collector current I_{C1} of Q_1 and assuming $I_{B2} << I_{C1}$, determine the collector current I_{C2} of Q_2. Determine V_{CE1} and V_{CE2} and hence verify that the BJTs are in active mode. [5]

A3.2.2 Identify the transistor configuration for each BJT and hence draw an ac small-signal equivalent circuit for this amplifier using appropriate models for the BJTs, assuming $V_T = 25\ mV$ and $V_A = \infty$. Determine the voltage gain $A_v \equiv v_o / v_{in}$ (in dB) assuming the capacitor reactances are negligible at signal frequencies. [5]

End of Analogue Electronics Section

DIGITAL ELECTRONICS – answer in a separate book **ANSWER ALL QUESTIONS**

Question D1 [25 marks]

D1.1 Write down the truth table for the circuit in figure D1 below. Hence, implement the circuit with a multiplexer. [6]

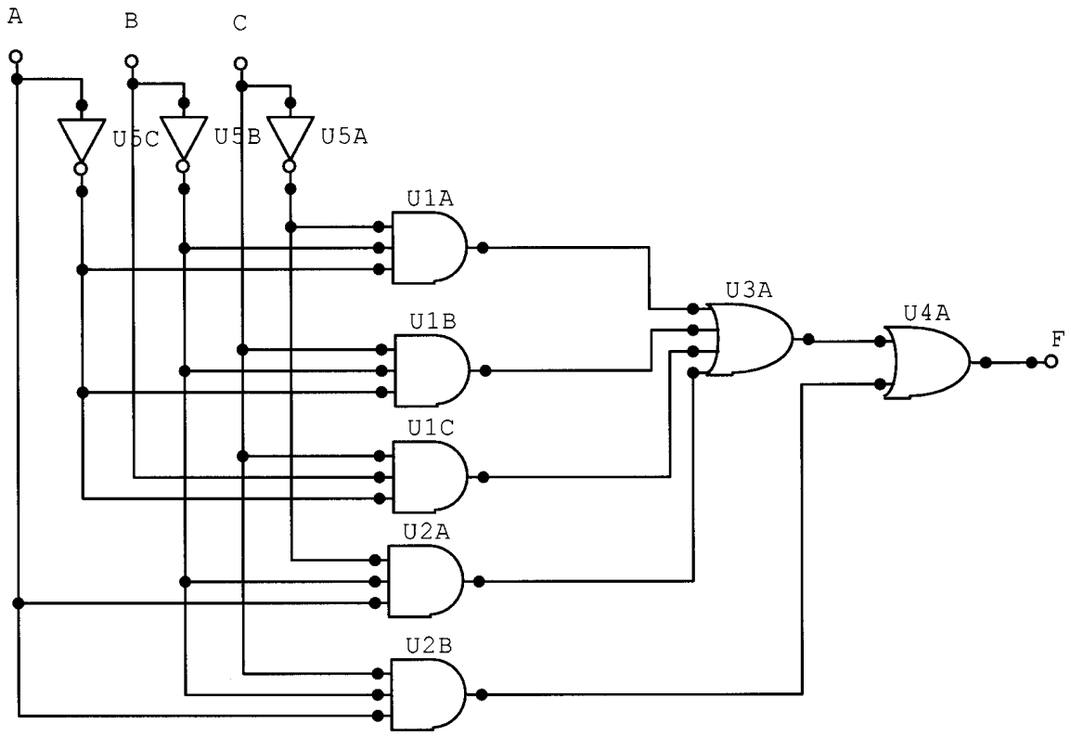

Figure D1

D1.2 The circuit in figure D2 represents an equivalent circuit to a logic gate where "A" and "B" are the inputs and "Y" is the output. Name the gate which it represents and with the aid of a truth table describe how the circuit in figure D2 works. [4]

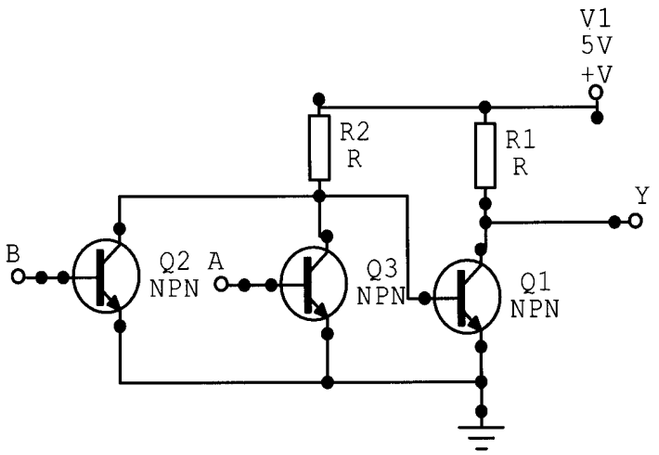

Figure D2

D1.3 Figure D3 shows a J-K flip-flop based *master-slave* circuit. With the aid of transition tables, describe how the circuit works and explain why it is necessary to have such circuits in some digital circuits. [6]

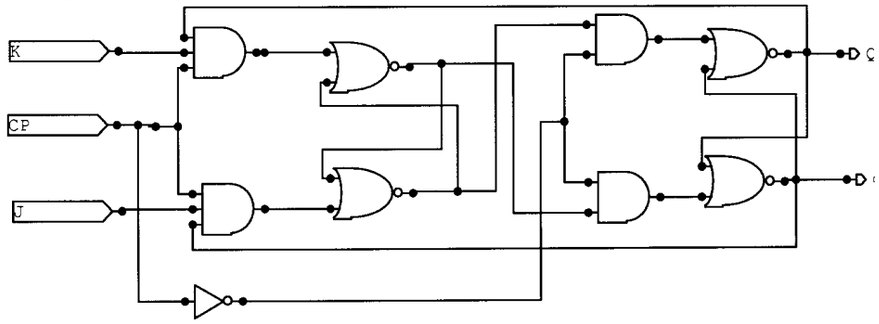

Figure D3

D1.4 Figure D4 below shows a 4-bit shift register. If the input 4-bit word, x = 1010, is to be loaded, draw the corresponding *state transition* and the *timing diagrams*. [4]

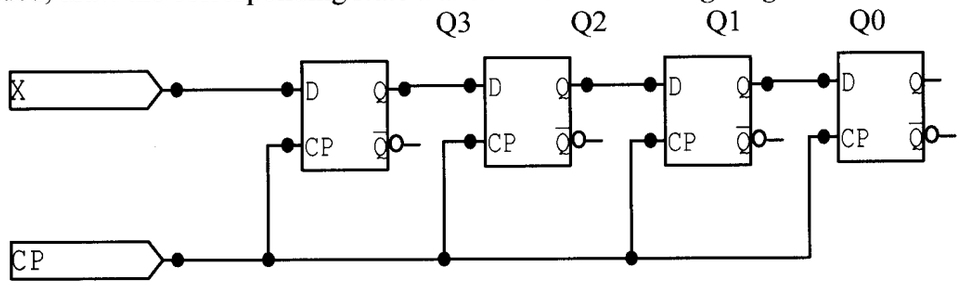

Figure D4

D1.5 With the aid of relevant diagram(s), describe the principles of operation of R-2R ladder *DAC* (digital to analogue converter). Given that, the reference voltage is 10V, calculate the output voltage of a three-bit R-2R ladder network if $S_0 = 1$, $S_1 = 0$ and $S_2 = 1$. [5]

Question D2: [25 marks]

D2.1 Implement the following Boolean function with a Multiplexer: [3]
$F(A,B,C,D) = \prod(1,2,3,5,6,8,9,10,13)$.

D2.2 Using MSI chips of your choice and some logic gates; design a system that counts continuously from 12 to 57 and display the count on a pair of 7-segment LEDs.
You should: [8]

i. State any assumptions made in your design.
ii. Give a complete block diagram of the system.
iii. Give brief explanation on how the system works.

D2.3 Design a system, which lights twelve LEDs in a **cyclic** sequence. Each LED lights for three seconds then goes off. You should: [5]

i. State any assumptions made in your design.
ii. Give a complete block diagram of the system.
iii. Give brief explanation on how the system works.

D2.4 The Table T1 below shows a truth table for a decade counter. The Q_i represent the normal output or state of a particular flip-flop. Use this table to derive the logic circuit for a decade counter and draw the circuit diagram. [9]

Table T1

Decimal count	Present Sate	Next Sate	Flip-Flop Input			
	$Q_3Q_2Q_1Q_0$	$Q_3Q_2Q_1Q_0$	J_3K_3	J_2K_2	J_1K_1	J_0K_0
0	0000	0001	0d	0d	0d	1d
1	0001	0010	0d	0d	1d	d1
2	0010	0011	0d	0d	d0	1d
3	0011	0100	0d	1d	d1	d1
4	0100	0101	0d	d0	0d	1d
5	0101	0110	0d	d0	1d	d1
6	0110	0111	0d	d0	d0	1d
7	0111	1000	1d	d1	d1	d1
8	1000	1001	d0	0d	0d	1d
9	1001	0000	d1	0d	0d	d1
10	1010	dddd	dd	dd	dd	dd
11	1011	dddd	dd	dd	dd	dd
12	1100	dddd	dd	dd	dd	dd
13	1101	dddd	dd	dd	dd	dd
14	1110	dddd	dd	dd	dd	dd
15	1111	dddd	dd	dd	dd	dd

End of Digital Electronics Questions

End of Question paper