The Discipline of Electrical, Electronic & Computer Engineering

Main Examination: September 2015

Embedded Systems (ENEL4ESH2)

Duration: 2 hours **Total Marks: 70**

Examiners: **Internal** Mr. E. Bhero

External Prof Tania Hanekom

General Instructions:

1. Answer **all** questions.
2. You can use a scientific calculator, but clear all program memory.
3. Try to keep your sketches as clear and as readable as possible.
4. Data sheet extract of PIC 16F690 is provided

Question 1: (15 Marks)

a) Two nodes on an automotive CAN bus are both ready to transmit data but the bus is busy with a message from the headlight switch (HLS) node. The two nodes are the Brake light switch (BLS) and the left indicator switch (LIS) wishing to send messages with IDs 0x023 and 0x07B respectively. Sketch the bus signals from the last bit of the HLS message until only one node is sending. Briefly explain your reasoning in coming up with the sketch.

[5]

b) After designing an embedded system, the performance is not satisfactory for a particular application. In order to meet the required performance, the speed and performance must increase by 31%. If the memory is responsible for 81% of the delays, determine the required memory speed-up ratio to achieve this required minimum performance.

[5]

c) Three CPU performance enhancements are proposed with the following speedups and percentage of the code execution time affected:
Speedup1 = S1 = 10 Percentage1 = F1 = 20%
Speedup2 = S2 = 15 Percentage1 = F2 = 15%
Speedup3 = S3 = 30 Percentage1 = F3 = 10%
While all three enhancements are in place in the new design, each enhancement affects a different portion of the code and only one enhancement can be used at a time.
What is the resulting overall speedup?

[5]

Question 2: (15marks)

A single purpose dedicated processor is required that will produce a selected output as per the code loop in figure 1 below. (*go_i* is a binary input, the values are presented on the inputs *x_i* and *y_i*. The output is produced on output *d_o*).

```
0: int x, y;
1: while (1) {
2: while (!go_i);
3: x = x_i;
4: y = y_i;
5: while (x != y) {
6: if (x < y)
7: y = y - x; else
8: x = x - y; }
9: d_o = x; }
```

Figure 1

a) From the figure above, sketch the logical FSMD diagram for a single purpose processor.

[5]

b) Split the FSMD into two parts, the Controller and the Data-path. Show all the units in the data-path and all the control signals between the two parts. (*Do not simplify or optimize your processor)*

[10]

Question 3: (15marks)

NASA space agency wants to develop a space-mission robot called "Ultra-Curiosity (UC)". A hierarchical embedded computer system comprising of one master controller, which is connected to at least four independent slave units will control the UC. Each slave unit is connected to at least four sensors, which sense various environmental parameters such temperature, pressure and so forth. In order to improve the reliability of data sent back to earth, the system implements a voting system that works in the following way; when the master controller broadcast the parameter to be measured each slave unit will send its own measured value. The value sent by the majority slave units is the one sent back to earth.
Assuming you are the project leader for the UC mission, prepare a design brief to be presented to the technical staff. In your design brief include the following:

a) Labelled block diagram of the system.
b) The type of network connection(s) you are going to use in the UC robot and why you chose that network?
c) The type of Processor(s) you are going to use for your master controller and the slave units and reasons for selecting the chosen processor(s).
d) Write a pseudo code for the possible program running in the master controller.

e) The process design model you are going to use in developing the system and the reasons for choosing that process design model.
f) State any possible design improvements and/or constrains.

[3+2+3+3+2+2]

Question 4: (25 marks)

You are a projects engineer for a technology company called Newtech Engineering (Pty) Ltd. You have been asked by the engineering manager to design a simple Plant controller unit, which is based on PIC 16F690 Microcontroller. The Microcontroller will be connected to the following; Real Time Clock (DS 1307), an 8-bit memory chip, a personal computer (PC) and to the Plant. A sequence of control COMMANDS must be sent to both the Plant and PC after every two hours. These COMMANDS are stored sequentially in the 8-bit memory chip. The Microcontroller is connected to the DS1307 through the I^2C bus.
With reference to this design, answer the following questions:

a) Draw a labelled block diagram for the proposed design.

[5]

b) Draw a flow chart representing the program flow in the Microcontroller.

[5]

c) Write program code (*assembly language or C/C++ only*) for the following parts of the Microcontroller program:

i. Configure the Microcontroller for I^2C communication as a slave unit. *(You may assume that the DS1307 is a master unit, which sends time bytes every hour).*

[5]

ii. A sequence of instructions leading to a successful reception of one byte from the DS1307.

[2]

iii. Configure appropriate Microcontroller port as an input.

[3]

iv. A sequence of instructions to read a COMMAND from the 8-bit memory chip and send it to a PC. (*You may make any reasonable simplifying assumptions*).

[5]

End of Examination Questions